Type of Article (Original Article)

A Power-Efficient Pipelined based Clock Gating FIFO for a Dual Ported Memory Array

Author's Full Name (S.Dhanasekar[1], L.Jubair Ahmed[2], V.Govindaraj[3], S.Rajesh Ruban[4], P.Malin Bruntha[5], G.Valarmathi[6])

[1]Department of ECE, Associate Professor, Sri Eshwar College of Engineering, Coimbatore, 641202, India.

[2]Department of ECE, Professor, Akshaya College of Engineering and Technology, Coimbatore, 642109, India.

[3] Department of ECE, Assistant Professor, Dr.NGP Institute of technology, Coimbatore, 641048, India.

[4] Department of Mechanical, Assistant Professor, Karunya Institute of Technology and Sciences, Coimbatore, 641114, India.

[5] Department of ECE, Assistant Professor, Karunya Institute of Technology and Sciences, Coimbatore, 641114, India.

[6] Department of ECE, Assistant Professor, Sri Sairam Institute of Technology, Chennai, 600044, India.

*** Corresponding author, Email address: dhanasekar.sm@gmail.com**

Abstract

FIFO is a special type of buffer which controls the data flow between the sender and receiver. It is used to monitor the serial data flow and avoids mismatch conditions between them. In general, dual-ported memory cell array suffers from dynamic power

dissipation. In this research article, a 128 x 128-bit Synchronous First In First Out (FIFO) buffer is designed for dual-ported memory cell array with pipeline architecture using clock gating technique which reduces power dissipation significantly. The FIFO-based dual-ported memory cell array will store a large number of data and minimize the clock skew. A circular FIFO used in dual-ported memory is organized in a circular queue fashion with two pointers write and read. Conventional FIFO designs used more power and hardware area on the silicon chip. The FIFO-based pipelining and clock gating approach will improve throughput while reducing dynamic power. The proposed FIFO design is simulated and implemented using the Cadence-Encounter tool using 180nm and 45nm Technology. The parameters like power consumption, cell utilization, and clock frequency have been analyzed. The synchronous FIFO design reduces the area by 70.3%, power dissipation by 10.6%, and operates by the clock frequency up to 322 MHz.

Keywords: Synchronous FIFO, Pipeline, Clock Gating, Read, Write

1. Introduction

Today, Electronic devices and the size of their components are reducing consistently due to the customer demand for making nanodevices with high performance and reduced cost. Hence various researchers are functioning towards shortening the transistor size to make miniature IC (Nagendran & Subramaniyam, 2020; Subramaniyam & Mani 2022). Digitization will be overwhelming all disciplines of engineering, which creates more impact on wideband wireless communication for high-speed data transmission (Subramaniyam, 2018). In wideband wireless applications,

OFDM transceiver IC supports high-speed data transmission in wireless communication (Subramaniyam, Paul & Kulandaivel, 2019). FIFO is a data buffer, similar to that of a queue with a First-come First-served (FCFS) response. It is arranged by a series of flip-flops or read/write memory which can store the data and it is transferred from one clock domain to another clock domain based on the request.

Generally, a clock domain that supplies the data to FIFO is known as a write or input signal, similarly clock domain that reads data from FIFO is known as read or output signal (Yantchev, Huang & Josephs, 1995). (ShilpiMaurya, 2016) proposes a design of RTL Synthesizable 32-Bit FIFO memory which is having less storage capacity. A new reconfigurable 64 bit FIFO memory circuit for synchronous and asynchronous communication is proposed by (Hafeez & Ross, 2021) and operates by the clock frequency of 1 GHz which consumes 2mw of power. An Optimal FIFO design methodology based on input and output data transfer rate is designed by (Rafi & Venkateshwara Rao, 2014). FIFO has less data transmission. In CMOS 180nm technology, a novel effective asynchronous FIFO has been synthesized, with a maximum throughput rate 10.88Gbps at 340MHz operating frequency (Nguyen & Tran, 2014). A 28nm ultra-Low Power First-In-First-Out (FIFO) memory is designed for the Multi-Bio-Signal Sensing platforms which achieve less area and power (Hsu, Huang & Wu, 2018) Several FIFO memory designs are used in various applications which achieve low power has been studied (Chang, 2009; Chiu, 2010; Du, 2011; Chang, 2008).

For high-performance digital systems, low power design is a major concern. Designers are always expecting the optimized power in the circuits to attain their power constraints. Clock gating is one of the essential power reduction methods which is

preferred by many designers and it is consistently used in gate-level power synthesis tools. Clock-Gating is among the most extensively utilized VLSI power optimization techniques (Attaoui, 2021). The challenge of the clock gating technique is when and where to insert the clock gating in the digital circuits or VLSI circuits which helps to optimize the power. Clock gating is an effective technique that reduces the switching activity significantly (Srinivasana, 2015). The switching capacitance reduction in the clock network and switching activity occurring at the time of inactive states of the clock reduces the power. There are various clock gating techniques that optimize power has been studied (Prakash, 2013; Weng & Weng, 2012). The Clock gating technique is achieved using three different designs namely 1) Flip flop based design 2) Gate based design 3) Latch based design. (Sharma & Rana, 2013) proposed gate-based clock gating design which is more desirable than flip flop-based design or latch-based design when power is considered as a major constraint.

Several FIFO memory designs have been reviewed for attaining optimized power in digital circuits. The existing FIFO designs occupied more power and hardware area in the silicon chip. Hence, there is a necessity to implement a power-optimized FIFO design. A low power clock gating FIFO for dual-port memory has been proposed.

In this article, a novel 128 x 128-bit synchronous FIFO is designed and implemented in a dual-ported memory cell array by using pipelining and clock gating techniques. In low power design, dynamic power contributes to the major source of power consumption which is due to switching activity. The pipelining and clock gating technique based on FIFO will increase the throughput and reduces the dynamic power. In the clock gating technique AND gate-based clock, gating is used to reduce the glitching activity of the device (Jaiwal, Paul & Mahto, 2014). (Datta, 2021) introduces a

FIFO synchronizer with a time-domain crossover interface providing unidirectional and bidirectional data transfer with minimal clock frequency degradation. In this proposed work, the pipelining technique is used to reduce the cell count which in turn enhances the speed of operation ((Jeon & Seok, 2012). FPGA technology provides a more reliable and flexible platform to test digital electronics circuits (Subramaniyam & Jayabalan, 2018; Subramaniyam & Jayabalan, 2015).

This paper methodized the synchronous FIFO in Dual ported memory. The proposed pipelined-based clock gating synchronous FIFO is portrayed. In the analysis of the results, the 128-bit synchronous FIFO is compared with the existing FIFO design, which attains significant improvement in area and power.

2. Materials and Methods

2.1 Synchronous FIFO in Dual Ported Memory

In this article, a circular FIFO is designed with memory components that are arranged in a circular queue fashion with two pointers namely write and read (Zhao, 2011). The read and write pointer indicates the endpoint and start point of the circle. During read or write operation, these pointers will be incremented one after another. This buffer consists of two flags namely FULL and EMPTY. These flags are used to support whether the FIFO is EMPTY (cannot be read from) or FULL (cannot be written to). The Full and Empty flags generated in a circular FIFO buffer are shown in Fig.1 (Apperson, 2007). By using a circular FIFO, we can store a large amount of data compared to a linear FIFO. The write and read operations in the circular FIFO will be performed in the same as well as different locations. This circular FIFO is mainly used to represent the full and empty condition of the circuit (Yang & Kim, 2009). In the

conventional method, a large amount of data is stored in the dual-ported memory cell array using a circular buffer instead of a register file.

The dual-port RAM component is used to read and write the data at the same time. This special kind of RAM consists of two unidirectional data ports, namely an input port is used for writing data and an output port is used for reading data. The input and output ports will have their unique address and data buses (Kline & Xu, 2018). The read port and write port has two signals namely READ and WRITE. The READ signal is used to enable the data output and the WRITE signal will allow the writing of the data (Das & Basu, 2022). To write the data into a FIFO buffer, then first we have to enable the write to enable line, and then the data will be inserted through the write data line. After that, the inserted data will be written to the dual-port memory array and the written data address will be stored in the write pointer. Similarly, if you want to read the data then enable the reader to enable line, after that the read pointer goes to the dual-port memory array (Hafeez & Otoom, 2022). The read pointer will read the address of the data, and then the read data will be displayed in the reading data line (Dong, 2012). This is the basic operation of the synchronous FIFO with a dual-port memory array structure.

The dual-ported memory cell array architecture is described in this article. As the name specifies in dual port memory, one port is used for reading operation and another port is used for a write operation as shown in Fig.2. In synchronous FIFO both read and write operations perform only on the clock pulse by the rising edge. Initially, the buffer will be in an empty state, because no data is written into the FIFO buffer so the memory indicates an empty flag (Wei & Jin 2022). To write the data into the FIFO, switch on the write E-enable pin then the write operation will be performed in the FIFO buffer during

the rising edges of the clock. For the read operation switch on the read E-enable pin, then the read operation will be performed on the output side of the FIFO buffer (Zhao, 2013; Chelcea & Nowick, 2000; Sharma, 2012). Two pointers are used to store the address of the input and output data. In the FIFO buffer, the compare logic is used to compare both read and write pointers. Whenever the read pointer attains the write pointer then the FIFO buffer indicates memory is FULL, and in reverse write, pointer attains the read pointer then the FIFO buffer indicates memory is EMPTY (Huang & Chang, 2007; Ross, 2019).

In the existing Dual ported memory cell array the speed of reading and write operation was improved and accuracy of output was maintained but the power consumption is increased. Hence there is a requirement for designing a low-power dual-ported memory cell array (Wimer, 2012; Kaushik & Gulhane, 2013; Duzer, 1995). The proposed pipelined-based clock gating FIFO used in the Dual ported memory cell array reduces the power consumption.

3. Proposed Pipelined based Clock Gating in Synchronous FIFO

Pipelining technique is used to improve the performance of the computation circuits by which the execution time will be increased. In this proposed synchronous FIFO, flip-flops are used as a basic component in pipelining and data flow is synchronized during computation. The components used in the pipelining approach are selected with low latency, high throughput, and less power consumption. Pipelining is mainly used to predict an occurrence at a single clock cycle before it will produce the result. During prediction, a certain range of output values are set at the clock cycles and these new values are stored using flip-flops (usually D type flip-flop is used). They appear at the output on the next clock cycle when the occurrence actually occurs. The

latch-free clock gating method uses a simple AND & XOR gate is shown in Fig 3 and the simulated waveform for clock gating D flip flop is shown in Fig 4.

The XOR gate will activate or set when the D and Q values are different. The clock signal & XOR gate flow as input to AND gate. The gated clock (gclk) obtained by the AND gate output will flow as the input to the D flip flop. The output of the XOR gate is enabled at two different inputs and the clock cycle is also enabled at the rising pulse then only a gated clock (gclk) will be enabled. The gate clock has less number of cycles than the original clock. The proposed clock gating technique reduces the dynamic power and increases the throughput in Synchronous FIFO.

4. Results and Discussion

The proposed synchronous FIFO is implemented by the Cadence Encounter tool using 45nm & 180nm technology. The Functional simulation of 128 x 128-bit synchronous FIFO without and with the pipeline is shown in Fig.5 and Fig.6 respectively. The output waveform of 128 x 128 bit synchronous FIFO shows both full and empty conditions based on the circular FIFO buffer. Once the buffer is FULL then no data will be written into the FIFO buffer. In a normal case if any of the data can be read or write after the EMPTY or FULL indication in the FIFO buffer, then the buffer indicates FIFO is in overflow or underflow condition. Hence, this problem can be avoided by using circular FIFO with the help of a dual-ported memory cell array.

In the waveform counter, the pin denotes the number of data that is used to write in the FIFO buffer and the temp data pin denotes the number of data that will be popped (after read operation) from the synchronous FIFO buffer. From the simulation results, it is inferred that 128 x 128 synchronous FIFO without pipeline produces 2ns delay in the empty state whereas synchronous FIFO with pipeline has no delay. The proposed 128 x

128 synchronous FIFO is implemented using 45 nm technology occupies 14069 total counts of logic cells which attained less area and delay as compared to 180 nm technology synchronous FIFO. The RTL Diagram of Synchronous FIFO using 45 nm Technology is shown in Fig. 7.

Table 1 exhibits the performance comparison of various FIFOs. The Implementation of area, delay, and power parameters for conventional and proposed synchronous FIFO is shown in Fig. 8. The proposed 128-bit synchronous FIFO implemented using 45nm technology uses 25.2% less power and 59.1% less area as compared to the existing FIFO (Ross, 2019). The clock gating-based 128-bit FIFO obtain a 77.6% area reduction, 35.7% power consumption, and 75.7% less gate delay over the FIFO (Hsu, Huang & Wu, 2018). The proposed FIFO implemented using 180nm technology occupies 70.3% less area, consumes 10.6% low power, and reduces the gate delay by 38% when compared to the existing FIFO (Nguyen & Tran, 2014). Table 2 shows Hardware utilization of 128 x 128 bit Synchronous FIFO. The 128-bit Synchronous FIFO and clock gate-based Synchronous FIFO are also implemented using the FPGA chip named QUARTUS II device, which has 4608 memory bits of system gate capacity. As compared to the normal Synchronous FIFO, clock gating-based Synchronous FIFO occupies 11.1% fewer memory bits.

4.1 Physical Level Implementation of 128 x 128 Synchronous FIFO

The Metal-fill insertion is a manufacturability step at the advanced nodes. Metal fills are dummy fills of metal pieces to avoid minimum density problems as shown in Fig. 9. If density on-chip is less than specified values this can cause problems during chemical-mechanical planarization which in turn affect the planarity of subsequent

layers. This can cause dishing effect. As these are just dummy metal pieces, it has no impact on timing and cross-talk.

5. Conclusions

In this paper, the pipelining-based clock gating technique is introduced to obtain area efficiency and low power in the synchronous FIFO memory design normally used for multiple read and writes operations in a single clock domain. This work has discussed the relevance of FIFO in synchronization between input and output data. The synchronous FIFO is mainly used to avoid overflow and underflow conditions. It is done by using a full and empty flag in the buffer circuit. The proposed synchronous FIFO design implemented using the Cadence Encounter tool by 180nm and 45nm technology with the supply voltage of 1.8V and 1V respectively, has reduced power dissipation to 10.6%, and area to 70.3%. As compared to existing FIFO buffers, the proposed 128 bit synchronous FIFO has been attained less power and area, and it is operated by maximum clock frequency up to 322 MHz.

References

Apperson, R. (2007). A Scalable Dual-Clock FIFO for Data Transfers between Arbitrary and Haltable Clock Domains. IEEE Transactions on Very Large Scale Integration (VLSI) systems, 15, 1125 – 1134.

Attaoui, Y., Chentouf, M. & Ismaili, Z, (2021). Clock Gating Efficiency and Impact on Power Optimization During Synthesis Flow. International Conference on Microelectronics (ICM). doi:10.1109/ICM52667.2021.9664896.

Chang, I. J. (2009). A 32 kb 10T Sub-Threshold SRAM Array With Bit- Interleaving and Differential Read Scheme in 90 nm CMOS. IEEE Journal of Solid-State Circuits, 650-658.

Chang, M. T. (2008). A Robust Ultra-Low Power Asynchronous FIFO Memory with Self-Adaptive Power Control. IEEE System-on-Chip Conference, 175-178.

Chiu, Y.T. (2010). Subthreshold Asynchronous FIFO Memory for Wireless Body Area Networks (WBANs). International Symposium on Medical Information and Communication Technology (ISMICT).

Chelcea, T., & Nowick, S.M. (2000). A low-latency FIFO for mixed-clock systems. Proceeding IEEE Computer Society workshop on VLSI, 119–126.

Das, S., & Basu, U. (2022). FPGA Implementation of Asynchronous FIFO. Proceedings of International Conference on Industrial Instrumentation and Control, 399–407. doi:https://doi.org/10.1007/978-981-16-7011-4_39

Datta, G. & Lin, S. (2021). High Performance and Robust FIFO Synchronizer-Interface for Crossing Clock Domains in SFQ Logic. IEEE Transactions on Circuits and Systems-II. doi: https://doi.org/10.48550/arXiv.2108.03719

Du, W. H. (2011). An Energy-Efficient 10T SRAM-based FIFO Memory Operating in Near-/Sub-threshold Regions. IEEE System-on-Chip Conference, 19-23.

Dong, X. (2012). NVSim: A circuit-level performance, energy, and area model for emerging nonvolatile memory. IEEE Transactions on Computer -Aided Design of Integrated Circuits and Systems, 31, 994–1007.

Duzer, T. (1995). Hybrid Josephson-CMOS FIFO. IEEE Transactions on Applied Superconductivity, 5, 2648-2651.

Hafeez, S., & Otoom, S. (2022). Design of memory Alias Table based on the SRAM 8T-Cell. International journal of circuit theory and applications. doi:https://doi.org/10.1002/cta.3284

Hafeez, S., & Ross, A. (2021). Reconfigurable FIFO memory circuit for synchronous and asynchronous communication. International journal of circuit theory applications, 49, 938-952.

Huang, P. K., & Chang, C. (2007). Recursive Constructions of Parallel FIFO and LIFO Queues with Switched Delay Lines. IEEE Transactions on Information Theory, 53, 1778-1798.

Hsu, W., Huang, P., & Wu, S. (2016). 28nm Ultra-Low Power Near-/Sub-threshold First-In-First-Out (FIFO) Memory for Multi-Bio-Signal Sensing Platforms. International Symposium on VLSI Design, Automation and Test (VLSI-DAT). doi: 10.1109/VLSI-DAT.2016.7482551

Jaiswal, R., Paul, R., & Mahto, V. (2014). Power Reduction in CMOS Technology by using Tri-State Buffer and Clock Gating. International Journal of Advanced Research in Computer Engineering & Technology (IJARCET), 3, 1853-1860.

Jeon, D., & Seok, M. (2012). A Super-pipelined Energy Efficient Subthreshold 240 MS/s FFT Core in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 47, 23-34.

Kaushik, P., & Gulhane, S. (2013). Dynamic Power Reduction of Digital Circuits by Clock Gating. International Journal of Advancements in Technology, 4, 79-88

Kline, D., & Xu, H. (2018). Racetrack Queues for Extremely Low-Energy FIFOs. IEEE Transactions on Very Large Scale Integration (VLSI) systems, 26, 1531- 1544.

Nagendran, A., & Subramaniyam, D. (2020). An Ultra-low-power Static Random-Access Memory Cell Using Tunneling Field Effect Transistor. International journal of Engineering Transactions B: Applications, 33, 2215-2221.

Nguyen, T., & Tran, XT. (2014). A novel asynchronous first-in-first-out adapting to multi synchronous network-on-chips. International Conference on Advanced Technologies for Communications. doi:10.1109/ATC.2014.7043413

Prakash, N. (2013). Clock Gating for Dynamic Power Reduction in Synchronous Circuits. International Journal of Engineering Trends and Technology, 4(5).

Rafi, S., & Venkateshwara Rao, K. (2014). FIFO Design Methodology Based on Input and Output Data Transfer Rate. Third National Conference on Latest Trends in Signal Processing, VLSI and Embedded Systems, 133-135.

Ross, A. (2019). A One-Cycle FIFO Buffer for Memory Management Units in Manycore Systems. IEEE Computer Society Annual Symposium on VLSI (ISVLSI). doi:10.1109/ISVLSI.2019.00056

Sharma, D. (2012). Effects of Different Clock Gating Techniques on Design. International Journal of Scientific & Engineering Research, 3.

Sharma, H., & Rana, C. (2013). Designing of 8-bit Synchronous FIFO Memory using Register File. International Journal of Computer Applications, 63, 23-26.

ShilpiMaurya, (2016). Design of RTL Synthesizable 32-Bit FIFO Memory. International Journal of Engineering Research & Technology, 5, 591-593.

Srinivasana, N. (2015). Power Reduction by Clock Gating Technique. Procedia Technology, 21, 631-635

Subramaniyam, D., & Jayabalan, R. (2018). VLSI Implementation of Variable Bit Rate OFDM Transceiver System with Multi-Radix FFT/IFFT Processor for wireless

applications. Journal of Electrical Engineering, 18, 2018- Edition: 1 – Article 18.1.22. ISSN:1582-4594.

Subramaniyam, D., & Jayabalan, R. (2015). FPGA Implementation of Variable Bit Rate 16 QAM Transceiver System. International Journal of Applied Engineering Research, 10, 26497-26507.

Subramaniyam, D. (2018). A Fast and Compact multiplier for Digital Signal Processors in sensor driven smart vehicles. International Journal of Mechanical Engineering and Technology, 9, 157–167.

Subramaniyam, D., Paul, M., & Kulandaivel, M. (2019). An Improved Area Efficient 16-QAM Transceiver Design using Vedic Multiplier for Wireless Applications. International Journal of Recent Technology and Engineering, 8, 4419-4425.

Subramaniyam, D., Mani J. (2022). Study of Polymer Matrix Composites for Electronics Applications. Journal of Nanomaterials, 2022, Article ID 8605099, 1-7. https://doi.org/10.1155/2022/8605099

Wei, H., & Jin, X. (2022). A Circuit Model for Working Memory Based on Hybrid Positive and Negative-Derivative Feedback Mechanism. Brain Sciences, 12(5), 547. doi:https://doi.org/10.3390/brainsci12050547

Weng, S., & Weng, H. (2012). Timing Optimization in Sequential Circuit by Exploiting Clock-Gating Logic. ACM Transactions on design automation of electronics systems, 17(2), 1-15.

Wimer, S. (2012). The Optimal Fan-Out of Clock Network for Power Minimization by Adaptive Gating. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 1772-1780.

Yang, H., & Kim, S. (2009). Low Power Input / Output Port Design Using Clock Gating technique. Recent advances in networking, VLSI and signal processing, 63-66.

Yantchev, T., Huang, C. G., & Josephs, M. B. (1995). Low latency asynchronous FIFO buffers. Proceedings second working conference on Asynchronous Design Methodologies, 24–31.

Zhao, W. (2011). Domain wall shift register-based reconfigurable logic. IEEE Transactions on Magnetics, 47(10), 2966–2969.

Zhao, W. (2013) Racetrack memory based reconfigurable computing. IEEE Faible Tension Faible Consommation, 1–4. doi: 10.1109/FTFC.2013.6577771

Figure

A Power-Efficient Pipelined based Clock Gating FIFO for a Dual Ported Memory Array

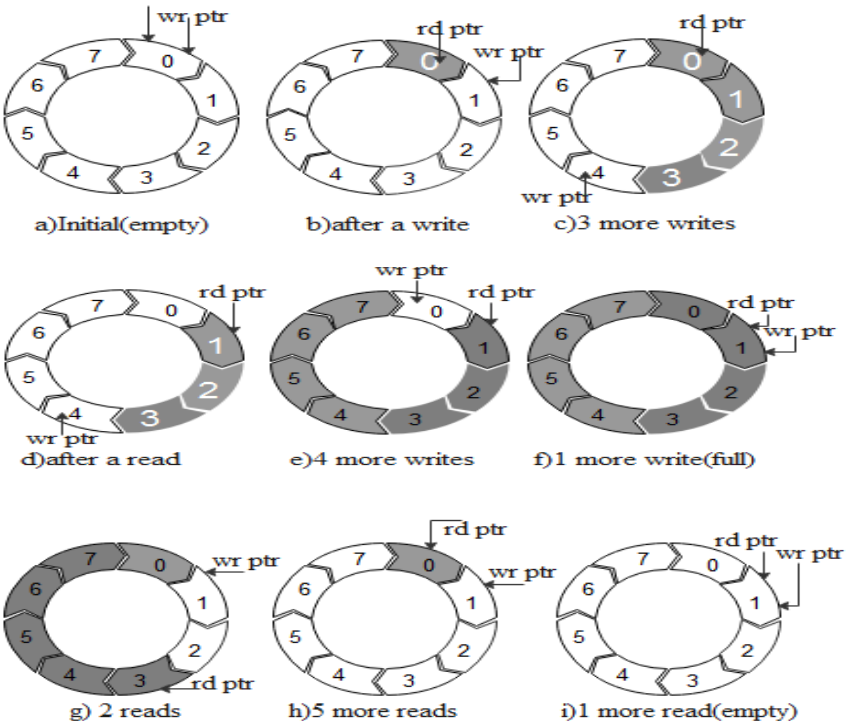

Fig. 1. Implementation of FIFO using circular buffer

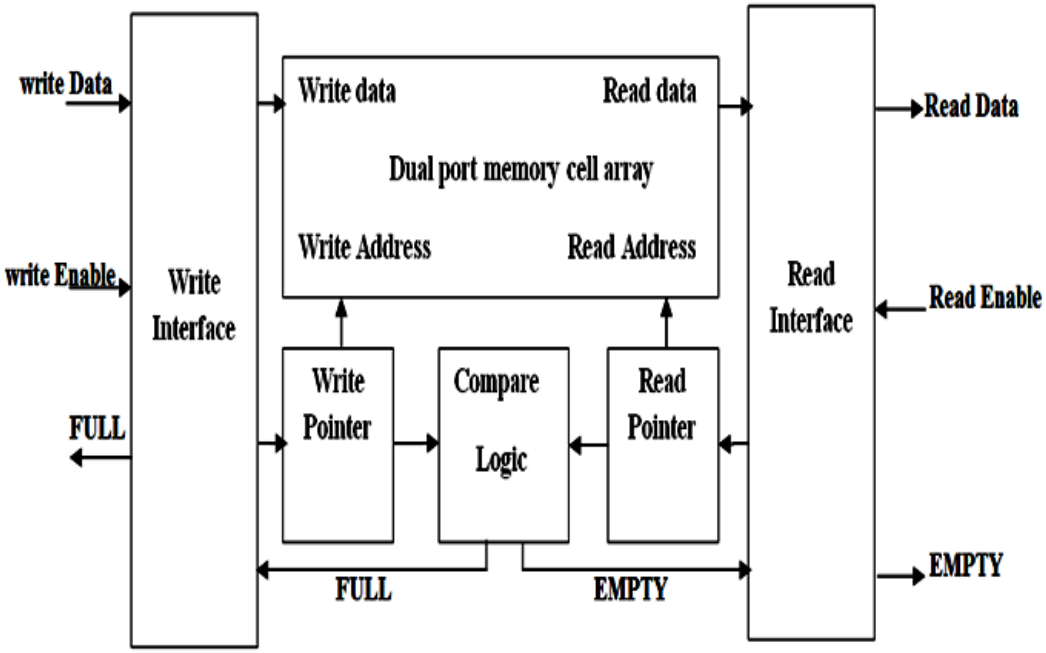

Fig. 2. Block diagram Synchronous FIFO with dual ported memory cell array

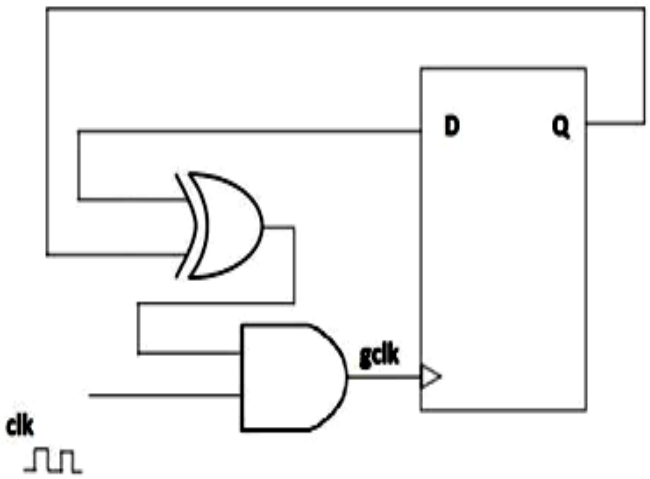

Fig. 3. Latch free clock gating D flipflop

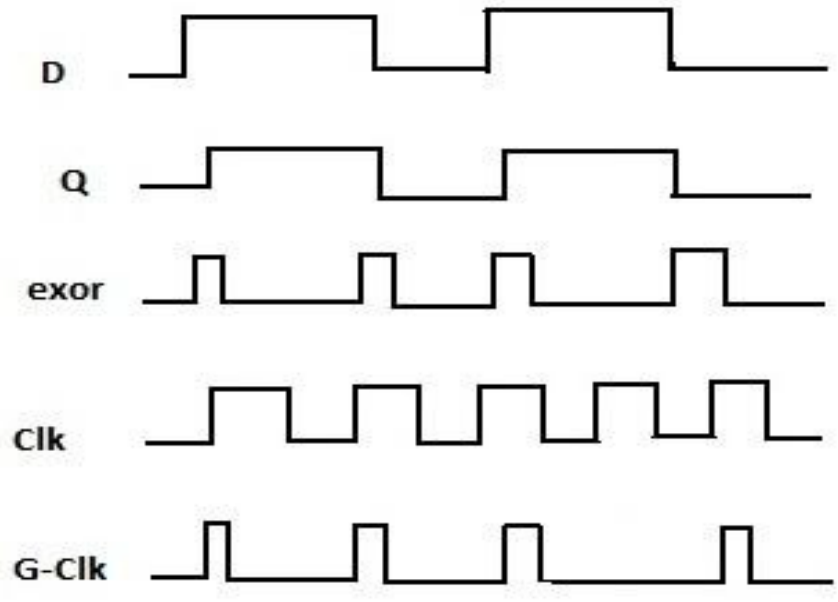

Fig. 4 Simulation waveforms for clock gating D flip flop

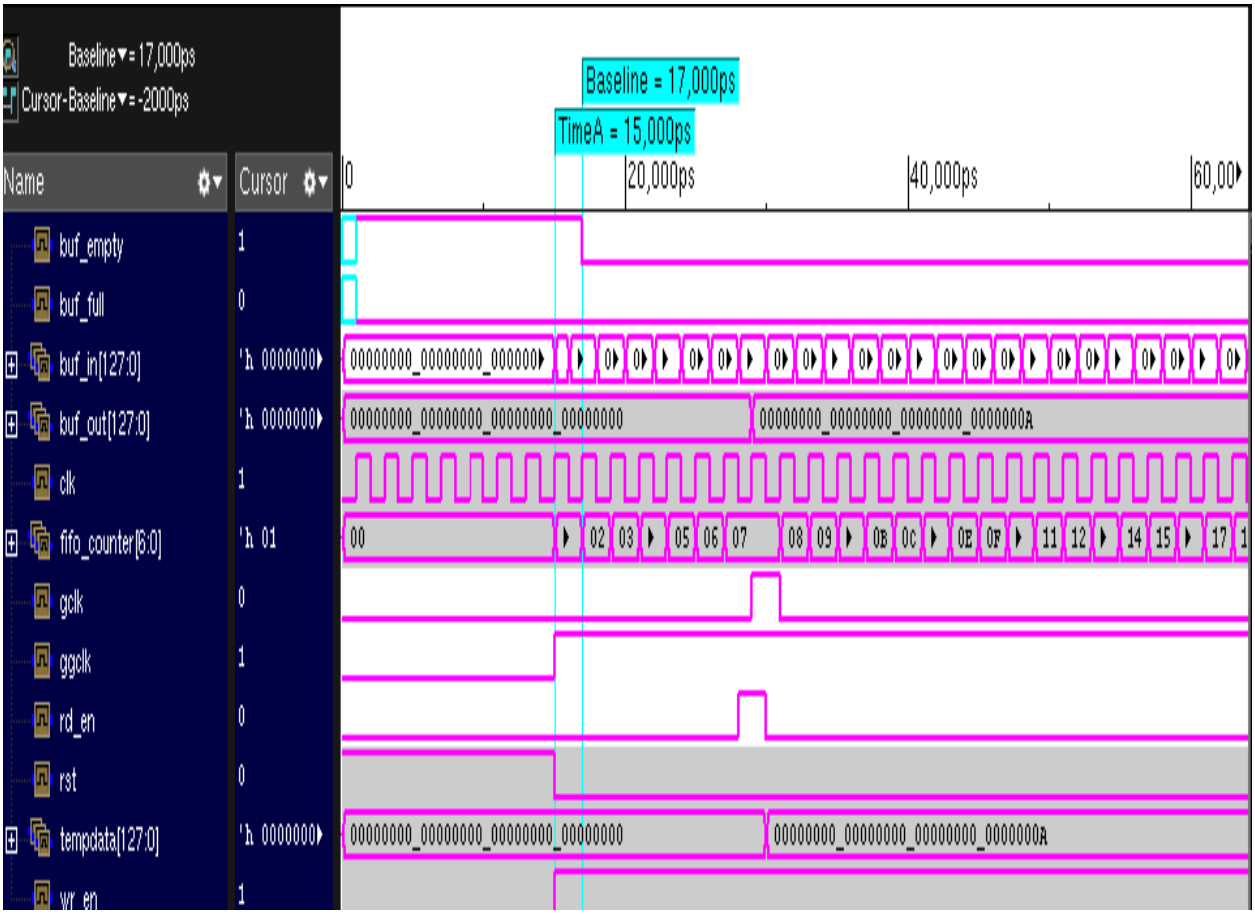

Fig.5. Simulation of 128 x 128 FIFO buffer in empty state without pipeline

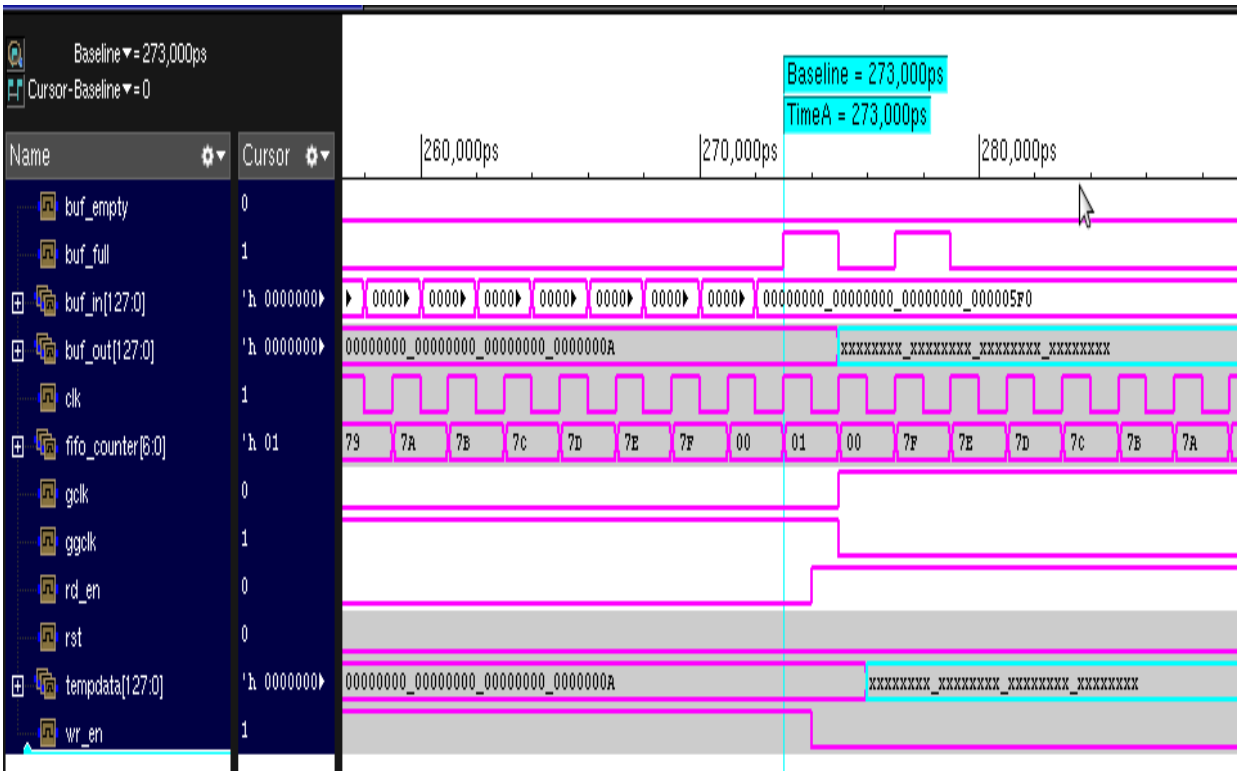

Fig.6. Simulation of 128 x 128 FIFO buffer in empty state with pipeline

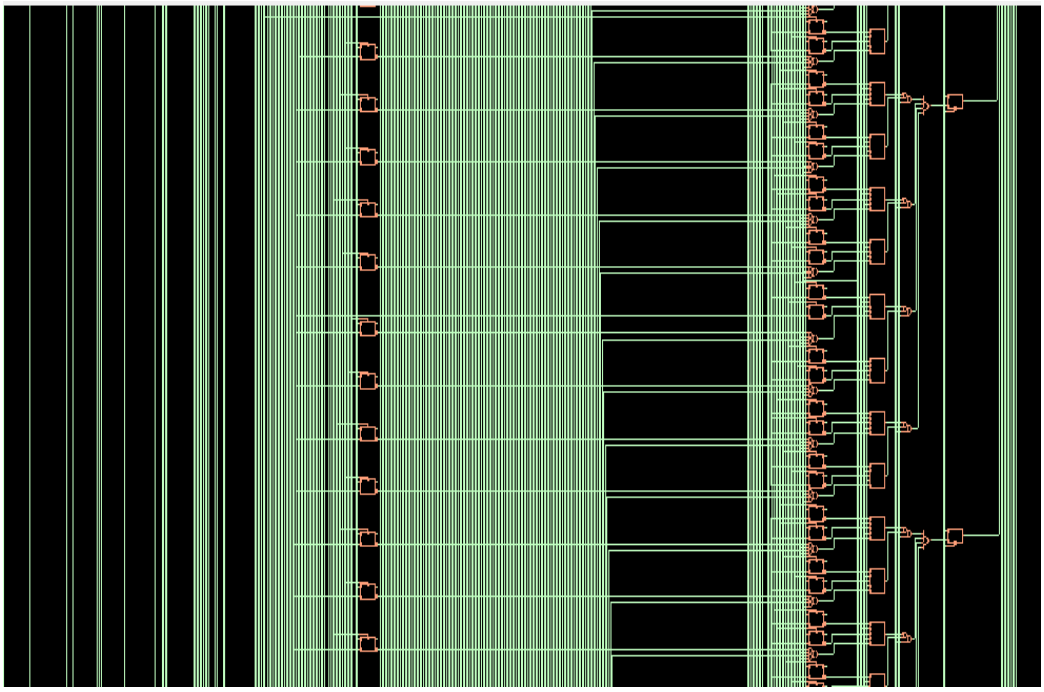

Fig. 7. RTL Diagram using 45nm Technology

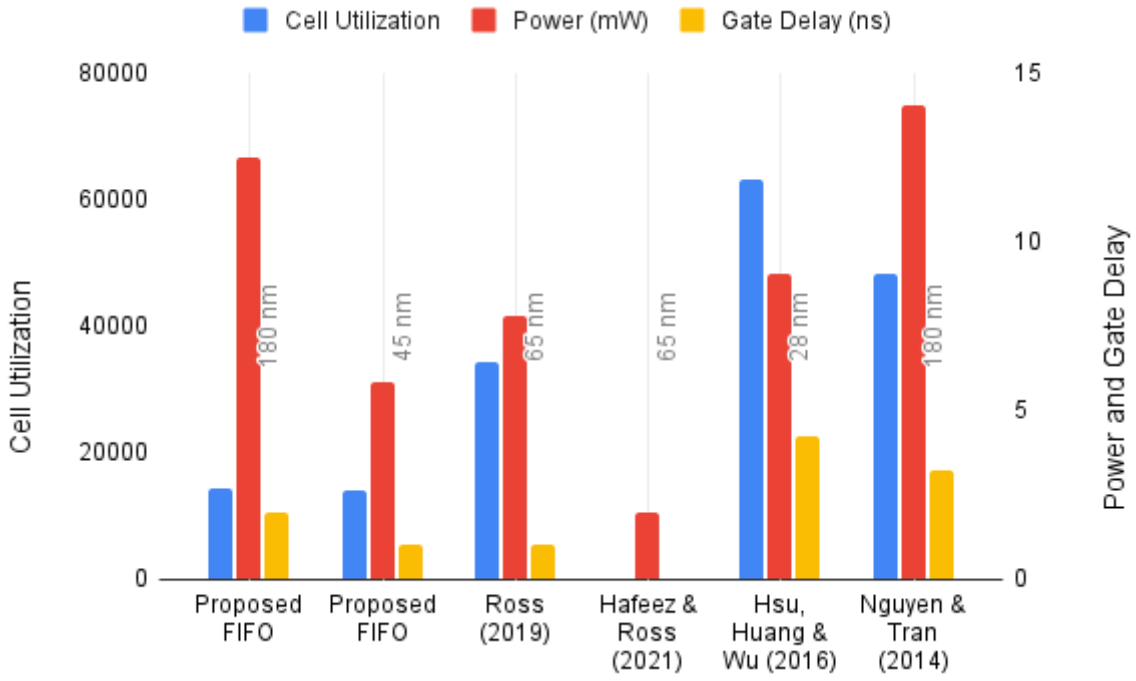

Fig. 8. Implementation of area, delay and power parameters for conventional and proposed synchronous FIFO

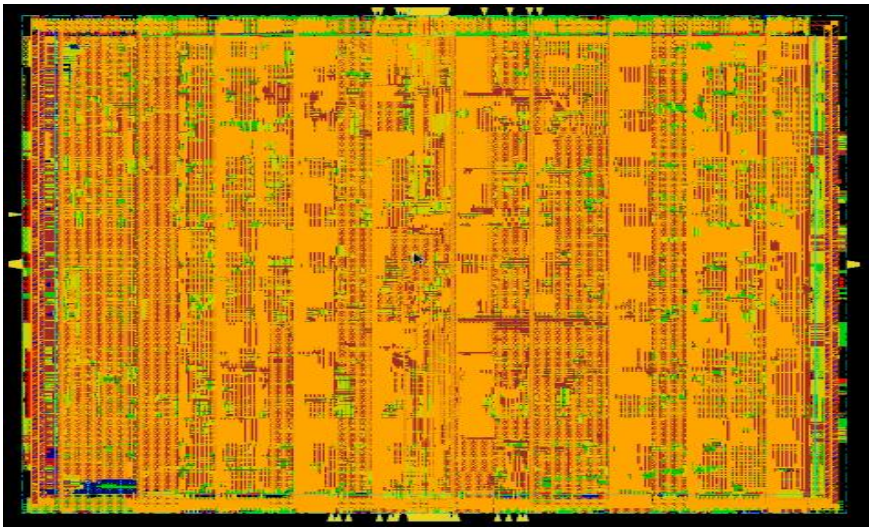

Fig.9. Metal fill of 128 x 128 bit synchronous FIFO buffer

Table

A Power-Efficient Pipelined based Clock Gating FIFO for a Dual Ported Memory Array

Parameters	Proposed FIFO	Proposed FIFO	Ross (2019)	Hafeez & Ross (2021)	Hsu, Huang & Wu (2018)	Nguyen & Tran (2014)
Technology	180 nm	45 nm	65 nm	65 nm	28 nm	180 nm
System Clock Frequency	322 MHz	324 MHz	1 GHz	1.15 GHz	10 MHz	340 MHz
Cell Utilization	14336	14069	34470	*	63083	48406
Power (mW)	12.53	5.83	7.8	2	9.07	14.025
Gate Delay (ns)	2	1.027	1.035	*	4.23	3.23

* denotes Not Reported

Table 1 Performance comparison of various FIFOs

*All entries are estimated values based on QUARTUS II synthesis tool for cyclone II Family and device name is EP2C70F89618

Number of Logic requirement	128 bit synchronous FIFO buffer	Proposed 128 bit Clocked gating Synchronous FIFO buffer
Number of Total combinational functions	192	158
Total number of registers	275	275
Total number of pins	270	270
Total number of memory bits	4608	4096

Table 2 Hardware utilization of 128 x 128 bit Synchronous FIFO