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Original Article

Fine tuning of cascaded d-q axis controller for AC-DC-AC converter without DC link capacitor using artificial neural network

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Abstract

This paper presents an artificial neural network (ANN) based approach to tune the parameters of the cascaded d-q axis controller for an AC-DC-AC converter without dc link capacitor. The proposed converter uses the cascaded d-q axis controller on the rectifier side and space vector pulse width modulation on the inverter side. The feed-forward ANN with the error back-propagation training is employed to tune the parameters of the cascaded d-q axis controller. The converter topology provides simple commutation procedure with reduced number of switches and has additional advantages such as good voltage transfer ratio, four quadrant operation, unity power factor, no DC link capacitor and less THD in both the line and load sides. Simulation results closely match with theoretical analysis.

Keywords: AC-DC-AC converter, back propagation algorithm, current source rectifier, neural networks, space vector modulation (SVM).

1. Introduction

Conventional AC-DC-AC converters are the indirect ac-ac converters widely used for power utility and drive applications. The active front end allows the converter to draw power nearer to the unity power factor as well as permitting regeneration of power into the supply. The performance of AC-DC-AC converter with dc link capacitor is presented in Mino, Okuma, and Kuroki, (1998) and Wei, and Lipo, (2001). The main draw back of this type of converter is the design of dc link capacitor for maintaining the desired ripple current rating. The method used to determine the dc link current drawn by an inverter is a complex numerical evaluation process (Evans, P.D. and Hill-Cottingham, R.J. 1986). Also the electrolytic capacitor introduces additional problems such as increased space and cost, and shorter life when compared to an ac capacitor (metalised polyester film) of the same rating. This limits the life and reliability of the inverter (Kenichi Limori, Katsuji Shinohara, Mitsuhiro Muroya and Yoichi Matsushita, 2002). Moreover the control aspects of pulse width modulation (PWM) techniques are much more complex due to commutation problem and it is difficult to improve the power factor on the line side. Hence researchers have focused on eliminating the DC capacitor in a traditional AC-DC-AC converter (Chan, Chau, and Chan, 1993 and Evans, and Hill-Cottingham, 1986) where the line side converter is a voltage source rectifier and the load side converter is a voltage source inverter. These circuits can effectively eliminate the DC side capacitor, but the line

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current contains a large amount of low order harmonics.

In this paper an attempt has been made to reduce the lower order harmonics in the line side by replacing the voltage source rectifier by a current source rectifier with a suitable modulation technique. This direct linked rectifier inverter without dc link capacitor has been developed in Matlab/Simulink using the blocks present in the power system tool box. The performance of the converter is analysed using pulse width modulation technique in the rectifier side and space vector modulation technique in the inverter side. An artificial neural network based cascaded d-q axis controller has been modeled to automatically adjust the control signal of the rectifier switches to fix the dc link voltage and current and to maintain unity power factor in the line side.

2. Proposed Topology

Figure 1 illustrates the structural view of the proposed AC-DC-AC converter without DC link capacitor (Cabell, Fuller, and Obrien, 1998) and (Lixiang and Lipo, 2003). Here the rectifier is assumed to be a current source rectifier, which is different from the conventional AC-DC-AC converter where the line side converter is a voltage source rectifier. The objective of the current source rectifier is to maintain a fixed DC voltage on the DC link without capacitor and improve the power factor on the input supply side. Now the capacitor in the DC link is replaced by an AC filter on the line side with a much smaller value to reduce higher order harmonics. Since converter has no large energy storage elements like a capacitor or an inductor it can be designed for higher capacity utilization. Since the fixed DC voltage is obtained at the DC link, inverter can be operated with any conventional modulation techniques but to obtain good voltage transfer and reduced distortion at the load side Space Vector Modulation method is preferred.

3. Analysis on Rectifier Side

For the analysis purpose switching frequency on the rectifier side is assumed to be far greater than the fundamental frequency of input voltage source. DC side voltage is essentially decided by the switching function of the rectifier and the input voltage. The input side voltages are assumed as:

$$V_{sx} = V_x$$
$$I_{sx} = I_x \text{ when } L_s = 0 \text{ and } C_f = 0 \quad (1)$$

where V_x is the line side voltage at converter side in phase x,
I_x is the phase current in the converter side,
x = a, b or c phase.

It is assumed that the input source voltages are three-phase balanced sinusoidal voltage sources, i.e.

$$V_{sa} = V_m \cos\theta_{av} = V_m \cos(\omega_i t)$$
$$V_{sb} = V_m \cos\theta_{bv} = V_m \cos(\omega_i t - \frac{2\pi}{3}) \quad (2)$$
$$V_{sc} = V_m \cos\theta_{cv} = V_m \cos(\omega_i t + \frac{2\pi}{3})$$

where V_m is the amplitude of the input phase voltage
θ_{av},θ_{bv} and θ_{cv} are the electric angles of phase A, B, C voltage.

The output currents are assumed to be a three-phase balanced sinusoidal current source then

$$I_U = I_o \cos\theta_{oi} = I_o \cos(\omega_o t + \varphi_o)$$
$$I_V = I_o \cos(\omega_o t + \varphi_o - \frac{2\pi}{3}) \quad (3)$$
$$I_W = I_o \cos(\omega_o t + \varphi_o + \frac{2\pi}{3})$$

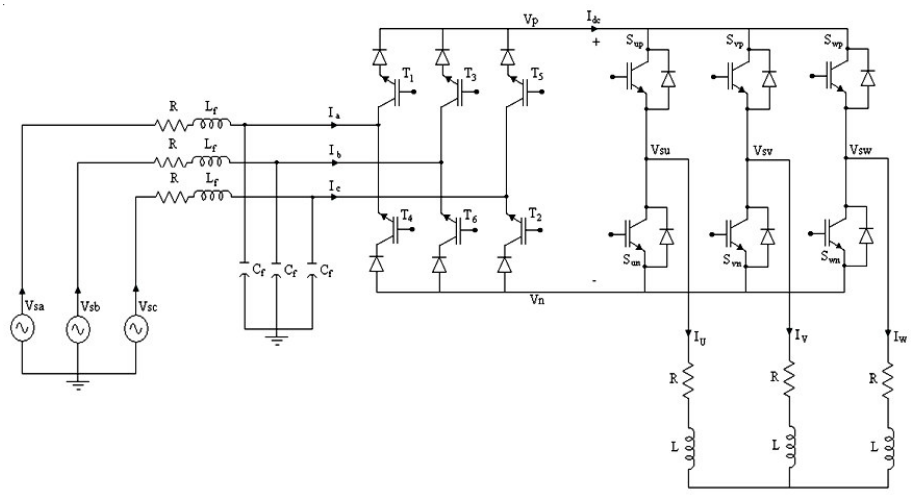

Figure 1. Topology of the proposed AC-DC-AC converter

where φ_o is the initital phase angle of the phase current
I_o is the amplitude of the output phase current

Moreover, the expected line side currents and load side fundamental output voltages are described as

$$I_a = I_m\cos\theta_a = I_m\cos(\omega_i t + \psi_{in})$$
$$I_b = I_m\cos\theta_b = I_m\cos(\omega_i t - \frac{2\pi}{3} - \Psi_{in}) \quad (4)$$
$$I_c = I_m\cos\theta_c = I_m\cos(\omega_i t + \frac{2\pi}{3} - \Psi_{in})$$

and

$$V_{su} = V_o\cos\theta_{ou} = V_o\cos(\omega_o t + \psi_{out})$$
$$V_{sv} = V_o\cos\theta_{ov} = V_o\cos(\theta_{ou} - \frac{2\pi}{3}) \quad (5)$$
$$V_{sw} = V_o\cos\theta_{ow} = V_o\cos(\theta_{ou} + \frac{2\pi}{3})$$

where $\psi_{in} = \theta_{av} - \theta_a$ is the line si de power factor angle
$\psi_{out} = \theta_{ou} - \theta_{oi}$ is the load si de power factor angle
θ_a, θ_b and θ_c are the electric phase angles of the line currents A, B and C
θ_{ou}, θ_{ov} and θ_{ow} are the electric phase angles of phase U, V and W voltages

From the above equations (2 to 5) it is clear that the input power factor is controlled by the factor ψ_{in} which provides from leading to unity power factor angle control (-30º to +30º) on the line side. Also on the load side the power factor is controlled by a factor ψ_{out}. To control the power factor on the line side and load side following PWM scheme is employed.

3.1 PWM Method on Rectifier Side

Analyzing the six intervals of a three phase sinusoidal voltage of a cycle, during each interval one of the line or phase voltages will have the maximum absolute value as shown in Figure 2. For example, in the interval 1, V_{sa} has the largest absolute voltage and in the interval 2, V_{sc} has the largest absolute voltage and so forth in all the intervals of

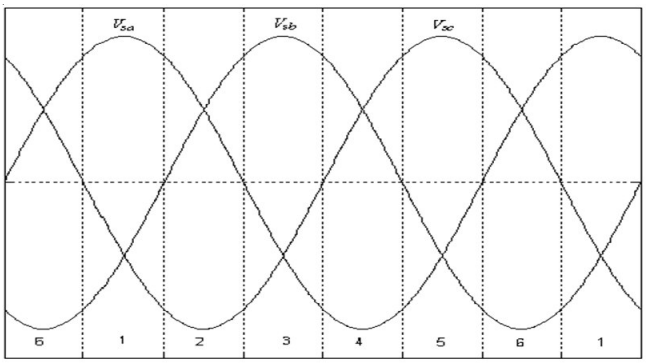

Figure 2. Six intervals of a switching cycle

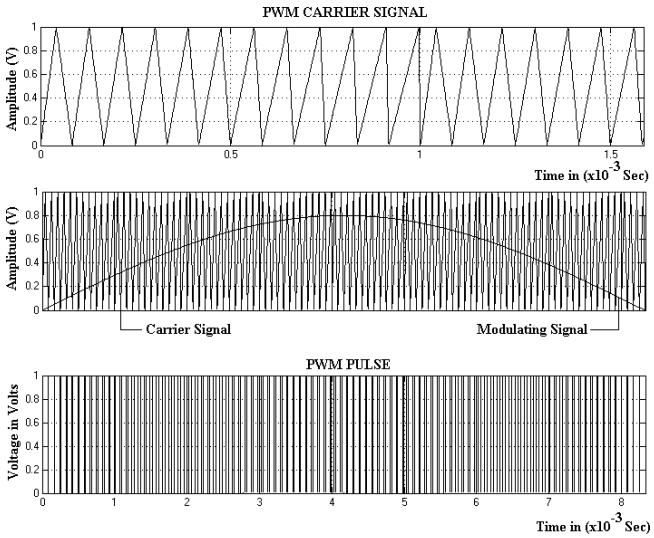

Figure 3. PWM scheme for Rectifier

the three phase sinusoidal voltage of a cycle. Each switching cycle is divided into two portions. PWM sequence on the rectifier side is developed by splitting each interval of conduction period into two portions, in which the largest absolute voltage corresponding to a particular switch will conduct for both the portions and one of the switches of opposite arm, adjacent to the leg will conduct in one portion and other switch will conduct in the second portion. For example, during interval 1, V_{sa} has the largest absolute voltage, with the corresponding line voltages V_{sa}-V_{sb} and V_{sa}-V_{sc}. In portion 1, for the first 30º conduction period T_1, T_6 remain turned on and all other line side switches are turned off. The DC side voltage V_{dc} is equal to V_{sa}-V_{sb}. In portion 2, for the next 30º conduction period T_1, T_2 remain turned on and all other line side switches are turned off. The DC side voltage V_{dc} is equal to V_{sa}-V_{sc}. The above sequence is applicable for all other intervals. By providing this switching sequence, DC voltage at the DC link can be maintained with a fixed value. Figure 3 illustrates the PWM scheme employed on the rectifier side. A special type of carrier is used which is initially triangular and then gradually changed to ramp. The main purpose of employing this type of carrier is to reduce the total harmonic distortion (THD) on the line side of the converter.

4. Cascaded d-q Axis Controller

In recent years the d-q transformation oriented closed loop controller are widely used in the power converter for their effective control on reactive power compensation and improving power factor. PWM technique using the cascaded d-q axis closed loop controller with ANN tuning is shown in Figure 4. The ac current control is considered particularly suitable for the rectifier due to its safety, stability performance and fast response (Kenichi Limori, Katsuji Shinohara and Kichiro Yamamoto, 1998). The controller structure is cascaded with the dc voltage controller because it calculates

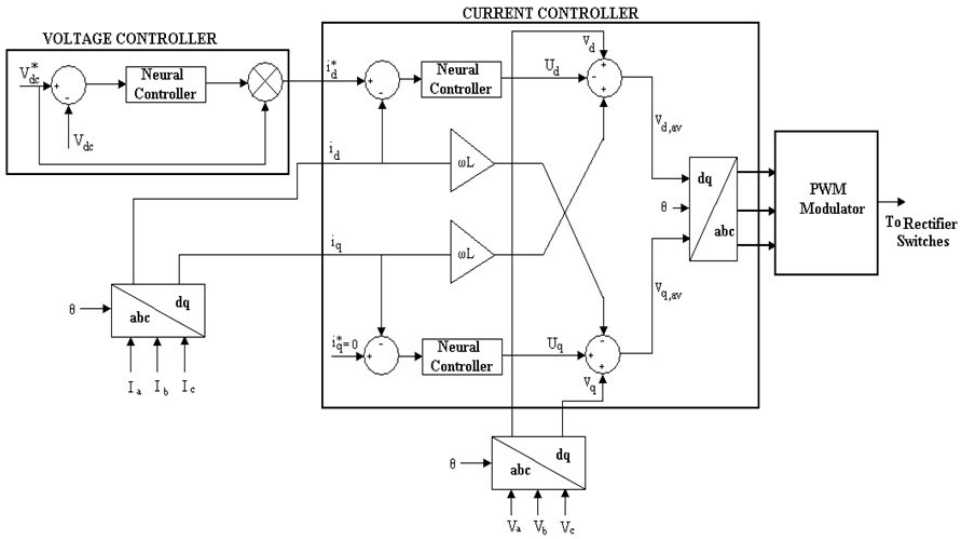

Figure 4. Cascaded d-q axis controller with ANN

the reference value for the d-axis current controller. Typic-ally, the inner current loops are atleast ten times faster than the outer loop controlling the dc voltage. To reduce the complexity of the PWM technique three phase voltages and currents are converted into two-phase quantities using Park's transformation to obtain d-q axis current and voltage for the controller. The reference DC voltage is compared with the actual DC link voltage to obtain the error. The error is fed to the neural controller to stabilize the error and to fix the DC link voltage. The reference d-axis current i_d^* is obtained from voltage controller and this is compared with actual d-axis current i_d and stabilized through neural controller to get the equivalent reference d-axis voltage U_d.

Similarly setting q-axis reference current $i_q^* = 0$ and the actual q-axis current i_q is compared and stabilized through neural controller to obtain the reference equivalent q-axis voltage U_q. The reference U_d and U_q are compared with actual V_d and V_q to obtain the equivalent average two phase quanities $V_{d,av}$ and $V_{q,av}$. The two-phase quantities are converted into three phase quantities using dq to abc trans-formation. This three-phase voltage is the control signal fed to the modulator for developing the switching pulse for rectifier side. The d-axis reference current i_d^* is controlled to perform the dc voltage regulation while the q-axis reference current i_q^* is typically controlled to obtain unity power factor using d-q cross compensation method and the controlling parameter such as i_d^*, U_d, U_q are tuned to the desired value using Back Propagation (BP) algorithm.

5. ANN Algorithm for d-q Controller

Neural networks with the abilities of real-time learn-ing, parallel computation, and self-organizing make pattern classification more suitable to handle complex classification problems through their learning and generalization abilities (Kim, Sul, and Lipo, 2000). An artificial neural-net (ANN)-based predictor was used along with a state predictor to greatly improve the performance of the rectifier regulator and shows a typical result where the impact of the prediction schemes on the dc-bus voltage ripple is obvious. The feed-forward ANN was trained on line using standard BP as opposed to most of the applications of the feed-forward neural nets where training is performed off line using pre-stored data. In general, each on-line training epoch consists of propagating the ANN input vector to compute its output, comparing this output with some reference to compute the training error, and finally modifying the ANN weights so as to reduce the magnitude of this error to obtain the optimum value. Similar training is done with all the patterns so that matching occurs for all the functions. This paper proposes and investigates the fast on-line training back propagation algorithm for feed-forward ANN.

5. 1 Back Propagation

Back propagation, which is the most popular training method for a multi-layer feed forward network is shown in Figure 5. The ANN with back propagation algorithm is

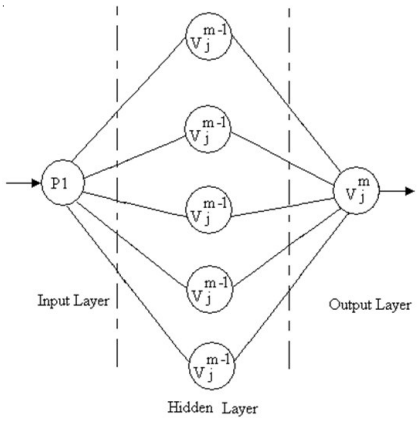

Figure 5. ANN architecture for tuning the d-q controller

trained with fifty thousand data for both voltage and current controlled part of the d-q controller. The topology is trained with one input layer, five hidden layers and one output layer with standard purelin, tansigmoid activation function. In Figure 5 the error data are set as PI vector and V_j^m are the corresponding output vectors, where m is the number of iterations. The vector V_j^{m-1} is the hidden layer activation function for the desired output.

5. 2 Back Propagation Algorithm

The input to the ANN is the error and the output is the desired proportional gain K_p and integral gain K_i for fixing the dc link voltage and current as well as to compensate the reactive power on the line side. The training data for the neural controllers are derived from the appropriate PI controller gain values for a typical load condition. The following steps are used for tuning the parameters of the d-q controller using BP algorithm.

1. Initially all the weights are set to small random value.

2. Present an input vector P and a desired output O apply I to the input layer (m = 0) so that $V^O = 1$.

3. For other layers, namely m = 1…….M, forward computation is performed using the equation (6)

$$V_i^{(m)} = f\left[\sum_i W_{ij}^m V_j^{m-1}\right] \quad (6)$$

where $W_{ij}^m V_j^{m-1}$ represent the connection weight from V_m^{m-1} to V_i^m.

4. The error is updated making use of the equation (7) and fed to the output layer

$$\delta_i^{(m)} = V_i^m(1-V_i^m)(O_i-V_i^m) \quad (7)$$

5. Then back propagation errors for the preceding layers M-1….1 are calculated using the equation (8)

$$\delta_i^{(m-1)} = V_i^{m-1}(1-V_i^{m-1})\sum_j W_{ji}^m \delta_j^m \quad (8)$$

6. Finally all the weights are adjusted for next iteration and is given by the equation (9)

$$W_{ij}^{(m)}(t+1) = W_{ij}^m(t) + \eta\delta_i^m V_j^{(m-1)} \quad (9)$$

where η is a gain parameter.

7. Repeat and go to step ii until the desired epoch is achieved.

6. Space Vector PWM for Inverter

The energy that a switching power converter delivers to a load is controlled by pulse width modulated signals applied to the gates of the power switches. The frequency of a PWM signal must be much higher than the fundamental frequency of the modulating signal, such that the energy delivered to the load and it depends mostly on the modulating signal. SVM is possibly the best PWM techniques for inverters. The inverter is analyzed as a voltage source inverter (VSI), the three-phase output voltages V_{su}, V_{sv} and V_{sw} are supplied by the DC voltage source which is fed from the line side fully controlled current source rectifier. Figure 6. shows the space vector PWM for inverter during the interval $0 < \theta < 60^0$ of the sector 1, where the output voltage $V = kV_m$. To overcome the commutation problem dead time has to be introduced by allowing zero vector before and after of the each conduction cycle. Using equation (10), the duty cycle of the conduction period has to be appropriately calculated for the switching sequences.

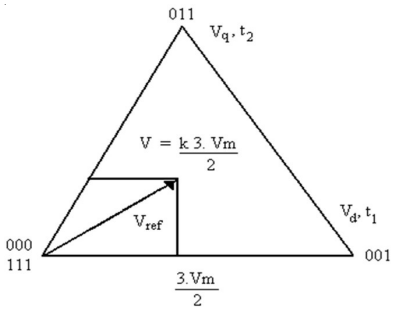

Figure 6. Space vector PWM for inverter during the instant $0 < \theta < 60^o$

$$T_1 = \frac{2}{\sqrt{3}}\frac{V_1}{V_2}T_c\sin(60-\theta_s)$$

$$T_2 = \frac{2}{\sqrt{3}}\frac{V_1}{V_2}T_c\sin\theta_s \quad (10)$$

$$T_0 = T_c - T_1 - T_2$$

7. Simulation Results

The proposed AC-DC-AC converter is analyzed using MATLAB/SIMULINK for its performance and all the switches used are ideal switches. The following simulation parameters are taken for analysis:

Line side parameters:

Input line voltage	= 220 V
Input frequency	= 60 Hz
Input filter resistance	= 0.2 Ω
Filter inductance	= 200 μH
Filter capacitance	= 900 μF

Load side parameters:

Output frequency	= 60 Hz
Load resistance	= 8
Load inductance	= 5 mH

Switching Frequency:

Modulation Index	= 0.8

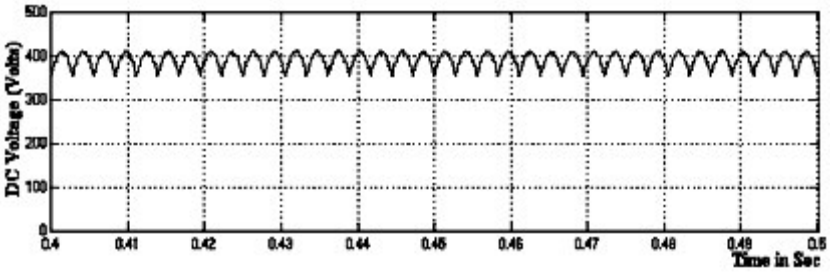

Figure 7. DC link voltage V_{dc}

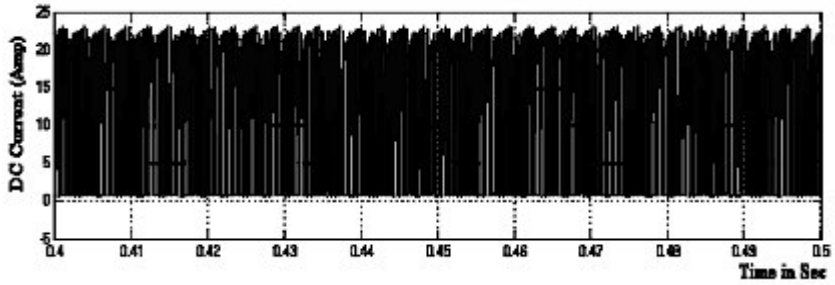

Figure 8. DC link current I_{dc}

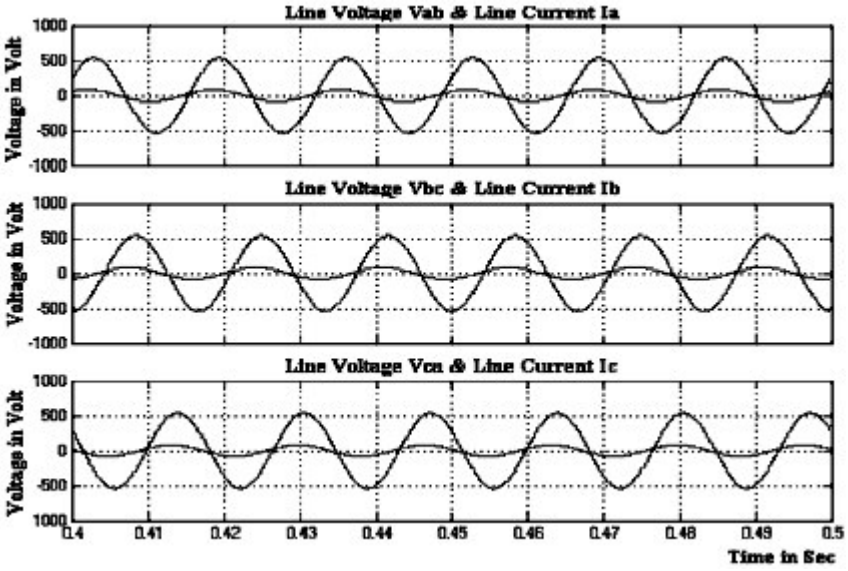

Figure 9. Line voltage and current (rectifier side)

Rectifier = 12 KHz
Inverter = 2 KHz

Figure 7 and Figure 8 show the dc voltage and dc current traces. These waveforms are modulated in each switching cycle maintaining a fixed dc voltage and current at the DC link. Figure 9 describes the waveform of three-phase voltage and current at the input side providing leading power factor. This result shows that at line side there are no lower order harmonics and all are suppressed by the filter. Figure 10 and Figure 11 depict that three phase output voltages (rms) and output currents (rms) are essentially sinusoidal. This in turn, demonstrates that there are no lower order harmonics in the output voltage and current. Figure 12 illustrates the total harmonic distortion at the rectifier side is about 4.36% with switching frequency of 12KHz. This shows that the PWM technique used on the rectifier side in suppressing the lower order harmonics thereby improving the fundamental components on the line side. Figure 13 show that the total harmonic distortion at the inverter side is about 22.79% with switching frequency of 2KHz without filter on the load side. This shows that lower order harmonics on the load side are also suppressed.

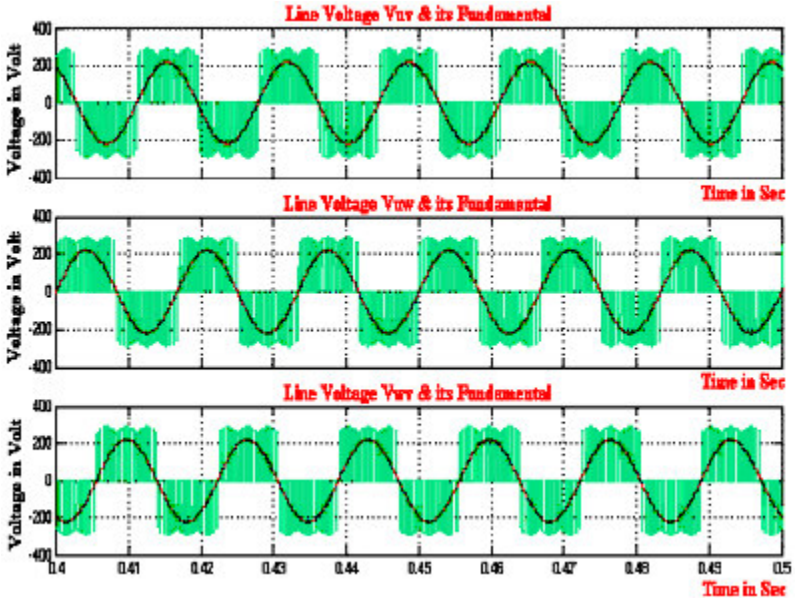

Figure 10. Load voltage and its fundamental (inverter side)

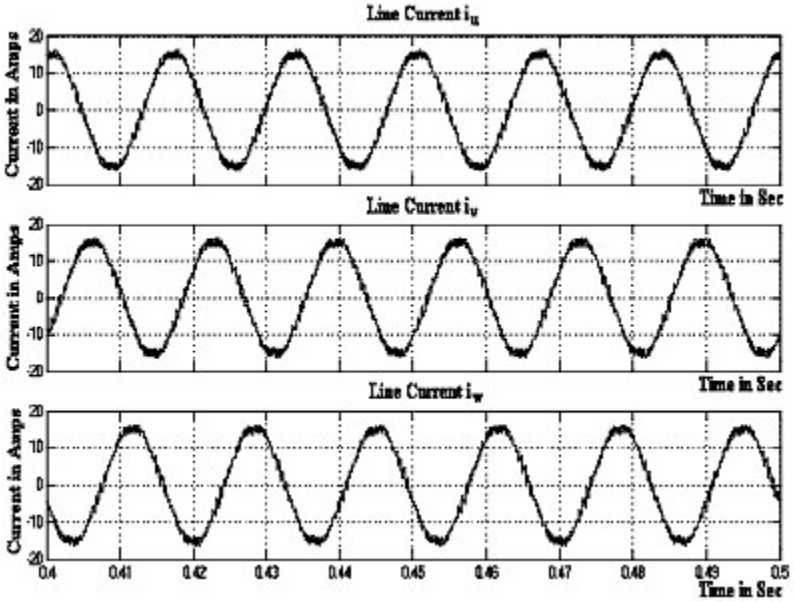

Figure 11. Load current showing sinusoidal characteristics

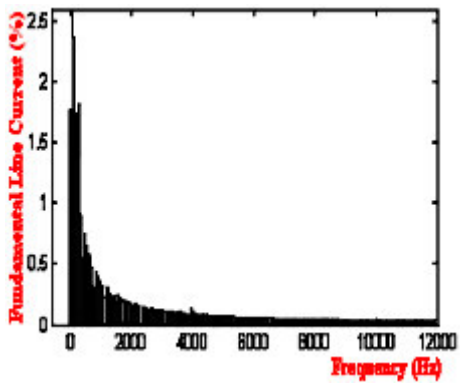

Figure 12. Harmonic analysis on the rectifier side

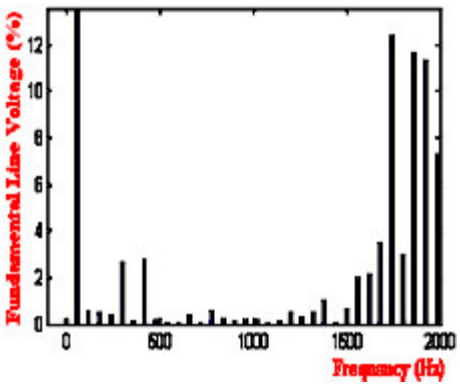

Figure 13. Harmonic analysis on the inverter side

8. Conclusion

This paper presents a successful application of neural network tuning method for the cascaded d-q axis controller present in the proposed AC-DC-AC converter topology. The neural network based d-q controller maintains the dc voltage and current at the dc link without dc link capacitor with reduced ripple current. Also the neural network controller provides unity power factor on the line side. Both the input current and output voltage are pure sine waveforms with only harmonics around or above the switching frequency. Hence filter requirement on both line and load side are reduced in size. The converter provides unity power factor at the line side and also improved power factor at the load side. Since DC link capacitor is eliminated, large capacity compact converter system can be designed. THD on the line side is 4.36% and on the load side is 22.79%. This implies that PWM methods analyzed provide feasible results. Space vector modulation is utilized for good voltage transfer from DC link and reduced distortion. From the performance analysis it can be concluded that the proposed converter is free from commutation problem and has better performance using ANN algorithm for compensating the reactive power and improved active power on the line side. The performances of this proposed converter are similar to the matrix converter and therefore it can also be treated as an alternative topology for matrix converter.

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